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| EXAMINER | |
|---|---|
| KIM, DAVID S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2633 | |

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/992,000 | KIKUCHI, OSAMU | |
| | Examiner | Art Unit | |
| | David S. Kim | 2633 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ ~~Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)~~ Paper No(s)/Mail Date *26 November 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ ~~Notice of Informal Patent Application (PTO-152)~~
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The foreign language references that have not been translated into English have been considered as best understood.

### *Drawings*

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitations must be shown or the feature(s) canceled from the claim(s):

(claim 13) a data detection circuit...

1. wherein the differentiation circuit differentiates the *second* amplified signal... (it appears that differentiation circuit 80 differentiates the *first* amplified signal in Fig. 7)

2. wherein the first comparator compares the *first amplified* signal with the fixed voltage...(it appears that comparator 81 compares the *differentiated* signal with the fixed voltage).

Please amend the drawings or the claims so that the limitations are properly shown in the claims. Additionally, no new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. **Claim 13** is objected to because of the following informalities:

In the last line, "preset" is used where -- present -- may be intended.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-3** are rejected under 35 U.S.C. 102(b) as being anticipated by Saito (U.S. Patent No. 5,822,104).

**Regarding claim 1**, Saito discloses:

An optical receiving apparatus, comprising:

a light receiving element (opto-electrical element 1 in Fig. 4) which converts an optical input signal into a corresponding electrical signal;

a pre-amplifier (pre-amplifier 3) having an input which receives the electrical signal from the light receiving element, a non-inverting output (output carrying Sbp) which outputs a first amplified signal, and an inverting output (output carrying Sbm) which outputs a second amplified signal which is phase inverted relative to the first amplified signal;

a data detection circuit (level detector 91) which receives at least one of the first and second amplified signals from the preamplifier, and which outputs a data detection signal in response to a change in a logic value of the at least one of the first and second amplified signals;

a reset circuit (reset pulse generator 92 and reset circuit 93) which receives the data detection signal from the data detection circuit, and which outputs a reset signal in response to a change in a logic value of the data detection signal; and

a threshold control circuit (automatic threshold circuit 5) which detects and outputs first and second peak values of the respective first and second amplified signals output from the pre-amplifier, wherein the threshold control circuit is responsive to the reset signal to remove a bias voltage (Fig. 5(e)) which is present in at least one of the first and second amplified signals.

**Regarding claim 2**, Saito discloses:

The optical receiving apparatus according to claim 1, wherein the threshold control circuit comprises:

a first peak hold circuit (first peak holding circuit 51) which outputs a first peak signal corresponding to a peak value of the first amplified signal; and

a second peak hold circuit (second peak holding circuit 52) which outputs a second peak signal corresponding to a peak value of the second amplified signal;

wherein the second peak hold circuit is responsive to the reset signal (signal from reset circuit 93) to remove the bias voltage from the second peak signal.

**Regarding claim 3**, Saito discloses:

The optical receiving apparatus according to claim 2 wherein the reset signal is a pulse signal having a given period (period of pulse in Fig. 5(d)), and wherein the given period of the reset signal is equal to or more than an amount of time needed by the second peak hold circuit to remove the bias voltage from the second amplified signal (note that signal Sem in Fig. 5(e) fully changes to match $-V_L$).

## *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Saito in view of the admitted prior art**

7. **Claims 4-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of the admitted prior art (hereinafter "APA").

**Regarding claim 4**, Saito discloses:

The optical receiving apparatus according to claim 2, wherein the threshold control circuit further comprises:

a first adder (first adder circuit 58) which adds the first amplified signal and the second peak signal; and

a second adder (second adder circuit 57) which adds the second amplified signal and the first peak signal.

Saito does not expressly disclose:

a differential amplifier which differentially amplifies respective outputs from the first and second adders.

However, optical receiving apparatuses commonly include such differential amplifiers. The APA discloses an exemplary differential amplifier (differential amplifier 25 in Applicant's Fig. 1). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate such a differential amplifier in the apparatus of Saito. One of

ordinary skill in the art would have been motivated to do this for the conventional benefit of differential amplifiers: to amplify a difference between two signals to a desired level, providing additional amplitude control to a practitioner of the apparatus of Saito.

**Regarding claim 5**, Saito in view of the APA discloses:

The optical receiving apparatus according to claim 4, further comprising a comparator (Saito, comparator 7) which discriminates an output of the differential amplifier with reference to a predetermined reference level (discriminating value Ls in Fig. 5(f)), and outputs an output signal (signal Sg).

**Saito in view of Nguyen et al.**

8. **Claims 6-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of Nguyen et al. (U.S. Patent No. 6,211,716 B1, hereinafter "Nguyen").

**Regarding claim 6**, claim 6 is a narrower version of claim 1. In particular, the limitations of claim 6 regarding the "data detection circuit" and the "reset circuit" include more structural details than corresponding limitations of claim 1 regarding the "data detection circuit" and the "reset circuit." As Saito is applied to address the limitations of claim 1, Saito discloses all the matching limitations of claim 6. Additionally, Saito also discloses the following narrower limitations of claim 6 regarding the "data detection circuit" and the "reset circuit":

a data detection circuit having a fixed voltage supply (V1), a first comparator (comparator 201) and a latch circuit (RS flip-flop 202), wherein the fixed voltage supply supplies a fixed voltage to the first comparator, and wherein the first comparator compares the first amplified signal (Sbp) with the fixed voltage, and wherein the latch circuit latches an output of the first comparator and outputs a first data detection signal (signal on the line to the upper port of EX-OR 204) and a second data detection signal (signal on the line to shift resistor 203); and

a reset circuit which receives the first and second data detection signals from the data detection circuit, and which outputs a reset signal (output from reset circuit 93) in response to the data detection circuit wherein the reset circuit includes a delay circuit (shift resistor 203) which delays one of the first and second data detection signals, and a logic circuit (EX-OR 204) which processes the other of the first and second data detection signals with an output of the delay circuit to obtain the reset signal.

Saito does not expressly disclose:

a second data detection signal *which is phase inverted relative to the first data detection signal*; and

a logic circuit which *multiplies* the other of the first and second data detection signals with an output of the delay circuit to obtain the reset signal.

Rather, Saito employs a slightly different apparatus to perform the functionally equivalent objective of obtaining a particular timing control signal, the reset signal. Nguyen teaches an apparatus that also performs the functionally equivalent objective of obtaining a particular timing control signal (Fig. 2D). The apparatus of Nguyen employs:

a second signal (signal input into upper port of AND gate 270) *which is phase inverted relative to a first signal* (signal input into lower port of AND gate 270, place inverter 265 before delay stage 260, such placement is trivially obvious and functionally equivalent); and

a logic circuit (AND gate 270) which *multiplies* the other of the first and second signals with an output of a delay circuit to obtain the particular timing control signal (230a).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the apparatus of Nguyen to perform the functionally equivalent objective of obtaining a particular timing control signal, the reset signal of Saito. One of ordinary skill in the art would have been motivated to do this since Saito teaches that the self-

reset circuit 9 may be constructed in any of other known circuit constructions (col. 8, l. 50-51); the apparatus of Nguyen constitutes such a suitable known circuit construction.

**Regarding claim 7**, Saito in view of Nguyen discloses:

The optical receiving apparatus according to claim 6, wherein the fixed voltage level (V1 in Fig. 7) is higher than a reference voltage level (0 in Fig. 5) of the first amplified signal.

**Regarding claim 8**, Saito in view of Nguyen discloses:

The optical receiving apparatus according to claim 6, wherein the reset signal is a pulse signal having a given period (period of S6 in Fig. 7), and the given period of the pulse signal is equal to an amount of time that the other of the data detection signals and the output of the delay circuit are simultaneously input into the logic circuit.

**Regarding claim 9**, Saito in view of Nguyen discloses:

The optical receiving apparatus according to claim 6, wherein the delay circuit delays one of the first and second data detection signals for a given period (period of pulse in Fig. 5(d)), and wherein the given period is equal to or more than an amount of time needed by the second peak hold circuit to remove the bias voltage from the second amplified signal (note that signal Sem in Fig. 5(e) fully changes to match $-V_L$).

**Regarding claim 10**, claim 10 is an apparatus claim that corresponds to apparatus claim 2. Therefore, the recited means in apparatus claim 2 read on the corresponding means in apparatus claim 10.

**Saito in view of Nguyen et al. and the admitted prior art**

9. **Claims 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of Nguyen as applied to claim 10 above, and further in view of the APA.

**Regarding claims 11-12**, claims 11 and 12 introduce limitations that correspond to the limitations introduced by claims 4 and 5, respectively. The APA is applied to address these

limitations in the treatment of claims 4-5 above. Similarly, the APA is applied to address these limitations in the treatment of claims 11-12 here.

**Saito in view of Nguyen et al. and Holcombe et al.**

10. **Claims 13-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of Nguyen et al. and Holcombe et al. (U.S. Patent No. 6,360,090 B1, hereinafter "Holcombe").

**Regarding claim 13**, claim 13 is similar to claim 6. In particular, the limitations of claim 13 regarding the "data detection circuit" include more structural details than corresponding limitations of claim 6 regarding the "data detection circuit." Additionally, the limitations of claim 13 regarding the "reset circuit" include less structural details than corresponding limitations of claim 6 regarding the "reset circuit." As Saito in view of Nguyen is applied to address the limitations of claim 6, Saito in view of Nguyen discloses all the matching limitations and broader limitations of claim 13.

However, Saito in view of Nguyen does not expressly disclose the following narrower limitations of claim 13 regarding the "data detection circuit":

a data detection circuit having a differentiation circuit, wherein the differentiation circuit differentiates the second amplified signal and outputs a differentiated signal.

Data detection circuits having differentiation circuits are known in the art. Holcombe teaches data detection circuits having differentiation circuits (Figs. 5 and 7). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to employ a differentiation circuit in the data detection circuit of Saito in view of Nguyen. One of ordinary skill in the art would have been motivated to do this to avoid the detection of noise pulses as valid pulses (Figs. 6 and 8), thus improving the sensitivity of the data detection circuit to detect

valid data transmissions instead of spurious noise as data transmissions. Additionally, Saito teaches that the self-reset circuit 9 may be constructed in any of other known circuit constructions (col. 8, l. 50-51); the incorporation of the differentiation circuit of Holcombe would still provide such a suitable known circuit construction.

Saito in view of Nguyen and Holcombe still does not expressly disclose:

wherein the differentiation circuit differentiates the *second* amplified signal.

Rather, Saito in view of Nguyen and Holcombe teaches that that the differentiation circuit differentiates the *first* amplified signal. However, applying the inventive self-reset circuit 9 of Saito, which may include said differentiated circuit of Saito in view of Nguyen and Holcombe, to the *second* amplified signal is an obvious variation of the apparatus of Saito in view of Nguyen and Holcombe; by inverting the appropriate logic components, one can provide the same functionality. Such inverting is usually technically trivial. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to arrange the apparatus of Saito in view of Nguyen and Holcombe to differentiate the *second* amplified signal. One of ordinary skill in the art would have been motivated to do this to provide design variety in the implementation and construction of the apparatus.

**Regarding claim 14**, claim 14 introduces limitations that correspond to the limitations introduced by claim 6. Saito and Nguyen are applied to address these limitations in the treatment of claim 6 above. Similarly, Saito and Nguyen are applied to address these limitations in the treatment of claim 14 here.

**Regarding claim 15**, Saito in view of Nguyen and Holcombe does not expressly disclose:

The optical receiving apparatus according to claim 13, wherein an initial voltage level of the differentiated signal is higher than the fixed voltage level.

However, in view of the obviousness argument presented in the treatment of claim 13 above, consider Fig. 7 of Saito. Sbp corresponds to said *first* amplified signal. In order to detect data transmissions, the fixed voltage level is set at V1. This arrangement applies to the situation where the inventive self-reset circuit 9 of Saito is applied to the *first* amplified signal. In the case where the inventive self-reset circuit 9 of Saito is applied to the *second* amplified signal, Sbm would become the signal of interest. Sbm is an inverted version of Sbp. Thus, to properly detect data transmissions, said fixed voltage level V1 would also be inverted. As such, an initial voltage level (initial level of Sbm) of the differentiated signal (Sbm) would be higher than the fixed voltage level (inverted V1).

**Regarding claim 16**, Saito in view of Nguyen and Holcombe discloses:

The optical receiving apparatus according to claim 13, wherein the first comparator outputs an output signal (the first comparator, by default, is always outputting an output signal) while the differentiated signal level is below the fixed voltage level (in another reading, consider the inverted version of S1 in Fig. 7).

**Regarding claims 17-18**, claims 17 and 18 are apparatus claims that correspond to apparatus claims 9 and 10, respectively. Therefore, the recited means in apparatus claims 9-10 read on the corresponding means in apparatus claims 17-18.

**Saito in view of Nguyen et al., Holcombe et al., and the admitted prior art**

11. **Claims 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of Nguyen and Holcombe as applied to claim 18 above, and further in view of the APA.

**Regarding claims 19-20**, claims 19 and 20 introduce limitations that correspond to the limitations introduced by claims 11 and 12, respectively. The APA is applied to address these limitations in the treatment of claims 11-12 above. Similarly, the APA is applied to address these limitations in the treatment of claims 19-20 here.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Saruwatari, Nagahori et al., and Mizunaga are cited to show related optical receiving apparatuses. Bonnefoy et al. is cited to show a related differentiation circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DSK

M. R. Sedighian

**M. R. SEDIGHIAN**
**PRIMARY EXAMINER**